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QUERY CONTROL FORM			RTIS USE ONLY	
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JACKET

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b. Applicant(s)	g. Disclaimer	l. Print Fig.	q. PTOL-85b
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d. PCT	i. Title	n. PTO-270/328	s. Sheets/Figs
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SPECIFICATION

a. Page Missing

b. Text Continuity

c. Holes through Data

d. Other Missing Text

e. Illegible Text

f. Duplicate Text

(g) Brief Description

h. Sequence Listing

i. Appendix

j. Amendments

k. Other

CLAIMS

a. Claim(s) Missing

b. Improper Dependency

c. Duplicate Numbers

d. Incorrect Numbering

e. Index Disagrees

f. Punctuation

g. Amendments

h. Bracketing

i. Missing Text

j. Duplicate Text

k. Other

MESSAGE

Please correct the type on line 5 of Page 4.
It should read Figure 8A not 8r

Thank You

initials TW

RESPONSE

Correction made.

initials JBH

E-5 (Rev. 10/01/02)

FIG. 6 is an enlarged cross-sectional view of an area "B" of the board of the board-mounted BGA package of FIG. 4;

FIGS. 7a to 7c are plan views illustrating several examples of enhanced pads of the present invention; and

5   FIGS. 8a to 8d are flow charts illustrating a method of mounting a BGA package on a board using the enhanced pads of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will be described below with
10   reference to the accompanying drawings. In particular, a board-mounted BGA package 200 according to an embodiment of the invention will be described in detail below with reference to FIGS. 4 through 6. FIG. 4 is a cross-sectional view of the board-mounted BGA package 200, including a chip 110 mounted on a substrate 120. FIG. 5 is a plan view of the bottom surface of the substrate 120 shown in FIG. 4. FIG. 6 is an enlarged cross-sectional view of an
15   area "B" of FIG. 4 showing an interconnection between a board 150 and the BGA package 200.

Referring to FIGS. 4 through 6, in the BGA package 200, the semiconductor chip 110 is mounted on the top surface of the substrate 120. Bonding pads 112 of the chip 110 are connected to metal wirings (not shown) of the substrate 120 via electrical connectors 130, such as bonding wires. The semiconductor chip 110 and the electrical connectors 130 are
20   encapsulated with a molding resin such as an epoxy molding compound (EMC), thereby forming a package body 140. Ball pads 124 are formed on the bottom surface of the substrate 120 and correspond to the metal wirings of the substrate 120. The ball pads 124 are exposed from, for example, a photo solder resist (PSR) layer 122. An external connection terminal
25   160 such as a solder ball is formed on each ball pad 124.

Enhanced pads 170 (including first, second, and third enhanced pads 170a, 170b, 170c) are preferably formed at outer edges of the bottom surface of the substrate 120. Each of the enhanced pads 170 comprises one ball pad 124, at least one dummy pad 174, and dummy patterns 172. The dummy patterns connect the ball pad 124 to the dummy pad 174.
30   The detailed structure of the enhanced pads 170 will now be further described.

The BGA package 200 is mounted on the board 150. The board 150 comprises ball lands 154 and enhanced lands 180, corresponding to the ball pads 124 and the enhanced pads 170. As shown in FIG. 6, the ball pads 124 and the enhanced pads 170b of the BGA package 200 are electrically connected to the ball lands 154 and the enhanced lands 180b of the board